REMARKS

This Amendment responds to the Office Action dated July 28, 2006 in which the Examiner rejected claims 1, 4-6, 10 and 13-17 under 35 U.S.C. §103.

As indicated above, claims 1, 6, 10 and 15 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claims 1, 6 and 10 claim an image processing apparatus and method in which an error diffusion processing is performed using a threshold value. In claims 1 and 10, error diffusion processing a) uses a single threshold value in a binarization process smaller than a single central value and b) does not perform calculation of error and distribution of the error for the white pixel. In claim 6, the error diffusion processing is performed using a single threshold value in a binarization process higher than a single central value.

Through the method and apparatus a) using a single threshold value which is either smaller or larger than a single central value and b) performing the error calculation based upon the input white signal, as claimed in claims 1, 6 and 10, the claimed invention provides an image processing apparatus which enables high speed image processing without degrading image quality. The prior art does not show, teach or suggest the invention as claimed in claims 1, 6 and 10.

Claim 15 claims an image processing apparatus including an error diffusion processing unit which outputs a signal representing a white or black pixel and does not perform calculation of error and subsequent distribution of errors to pixels when the input signal represents the white or black pixel. The error diffusion processing

unit performs error diffusion process using a single threshold value in a binarization process and changes the threshold value based on a relationship between the input and the threshold value. The relationship is that the threshold value increases depending on the increase of the input.

Through the structure of the claimed invention using a single threshold value in a binarization process, changing the threshold value based upon a relationship between the input and the threshold value such that the threshold value increases depending on the increase in the input, as claimed in claim 15, the claimed invention provides an image processing apparatus which enables high speed image processing without the degrading image quality. The prior art does not show, teach or suggest the invention as claimed in claim 15.

Claims 1, 4-6, 10 and 13-17 were rejected under 35 U.S.C. §103 as being unpatentable over *Ishiguro et al.* (U.S. Patent 6,501,566) in view of *Engineering Design Choice*.

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Ishiguro et al. appears to disclose an image processing apparatus employing a multi-value error diffusion process. (Column 1, lines 9-10). An error diffusion process is carried out, if necessary, by error diffusion processing unit 106-07. In the error diffusion process, pixel density D of the image data output from MTF correction unit 106-06 and a reference density S output from control unit 106-12 are used. Converted pixel density P of the image data subjected to an error diffusion process is

output from error diffusion processing unit 106-07. (Column 6, lines 23-30). FIG. 3 is a block diagram showing a structure of error diffusion processing unit 106-07 of FIG. 2. Referring to FIG. 3, an error diffusion processing unit 106-07 includes an adder 41, a tone convertor 42, a subtractor 43, an error addition matrix 44, an error memory 45, and an address counter 46. The function of respective blocks is similar to those described with reference to FIG. 10. Only differing portions will be described hereinafter. FIG. 4 is a block diagram of tone convertor 42. Referring to FIG. 4, tone convertor 42 includes average value circuits AVE1-AVE3, comparators CP1-CP3, a data selector SEL, and an encoder ENC. A reference density S is applied to each of average value circuits AVE1-AVE3 and data selector SEL. Reference density S is formed of reference densities S0-S3. Average value circuit AVE1 receives reference densities S0 and S1 to output the average value thereof as a threshold value T1. Average value circuit AVE2 receives reference densities S1 and S2 to output the average value thereof as a threshold value T2. Average value circuit AVE3 receives reference densities S2 and S3 to output the average value thereof as a threshold value T3. (Column 6, lines 38-63). The image processing apparatus of the present embodiment is characterized in that the values of reference densities S1 and S2 are altered according to the density histogram of the input image data. (Column 7, lines 13-16). Reference densities S1 and S2 set as described above and S0 (=0) and S3 (=255) which are the lower limit value and upper limit value, respectively, of the density value are applied to average value circuits AVE1-AVE3 and data selector SEL as shown in FIG. 4. Threshold values T1-T3 are calculated by averaging the reference densities in average value circuits AVE1-AVE3. According to threshold values T1-T3, corrected pixel density D' is compared in comparators CP1-CP3. The

result of the comparison is provided to encoder ENC. FIG. 8 is a list showing the relationship of corrected pixel density D', converted pixel density P output from encoder ENC, output Ti of data selector SEL, and error E output from subtractor 43 of the pixel of interest when reference density S1 is 85 and reference density S2 is 170. Referring to FIG. 8, the threshold values are T1=42, T2=127, and T3=212 since the reference densities are S0=0, S1=85, S2=170, and S3=255. Therefore, converted pixel density P is 00 when corrected pixel density D' is 0.about.41. Here, the value of SO, i.e., 0, is provided as output Ti of data selector SEL. Therefore, error E output from subtractor 43 is D'-0. (Column 8, lines 31-52).

Thus, *Ishiguro et al.* merely discloses in Fig. 3 performing an error diffusion processing even if an input signal D is zero. In other words, the input signal D is input to the adder 41 regardless of the value of the input signal D. The adder 41 adds a correction value R to the input signal D to generate a signal D' as corrected. The correction value R is an error generated from values of surrounding pixels. Therefore, if a pixel of a value other than zero is generated, the error would be diffused and thus zero is not readily reached. It is thus apparent that *Ishiguro et al.* performs the addition of the correction value R and subsequent error diffusion even if the input signal D is zero. Thus, nothing in *Ishiguro et al.* shows, teaches or suggests not performing calculation of an error and subsequent distribution of the error to pixels when the input signal represents a white pixel (i.e., zero) as claimed in claims 1, 10 and 15. Rather, *Ishiguro et al.* teaches away from the claimed invention and performs error diffusion process even if the input signal is zero.

Also, *Ishiguro et al.* merely discloses three threshold values T1, T2 and T3. However, as claimed in claims 1, 6, 10 and 15, only one threshold value is

determined in the binarization process. However, *Ishiguro et al.* discloses three threshold values depending upon the density level.

Additionally, *Ishiguro et al.* merely discloses average value circuit AVE1 receives reference densities S0 and S1 to output an average value thereof as a threshold value T1 and thus shows in Figure 7 that T1 is a central value of the reference densities S0 and S1. In other words, in the range in which certain binarization is performed by *Ishiguro et al.* (the range being S0 and S1), the threshold value is the central value and not any value larger or smaller than the central value. Thus, nothing in *Ishiguro et al.* shows, teaches or suggests using a single threshold value larger or smaller than a single central value as claimed in claims 1, 6 and 10. Rather, *Ishiguro et al.* teaches away from the claimed invention since the range on which binarization is performed by a *Ishiguro et al.*, the threshold value is the central value.

Furthermore, as discussed above, *Ishiguro et al.* only discloses the range on which certain binarization is performed (for example, the range between S0 and S1) and that the threshold value is the central value. Nothing in *Ishiguro et al.* shows, teaches or suggests that the threshold value may be changed to be smaller or larger as claimed in claim 15. Rather, *Ishiguro et al.* only discloses that the threshold value is the central value.

Applicant respectfully traverses the Examiner's statement that an obvious engineering design choice to not perform error and error distribution calculations when the input signal is a white pixel or a black pixel. Nothing in any of the references nor any provided information discloses why error and error distribution calculations would not be performed on white or black pixels. Column 9, lines 27-35

of *Ishiguro et al.* merely discloses setting the density ranges such as for a half tone density text. Furthermore, *Ishiguro et al.* teaches performing error diffusion processing even if the input signal is zero. Applicant respectfully requests the Examiner provide a reference showing why it would be obvious not to perform error and error distribution calculations for white or black pixels.

Since nothing in *Ishiguro et al.* or *Engineering Design Choice* shows, teaches or suggests the primary features as claimed in claims 1, 6, 10 and 15 as discussed above, Applicant respectfully requests the Examiner withdraws the rejection to claims 1, 6, 10 and 15 under 35 U.S.C. §103.

Claims 4-5, 13-14 and 16-17 depend from claims 1, 10 and 15 and recite additional features. Applicant respectfully submits that the claims 4-5, 13-14 and 16-17 would not have been obvious within the meaning of the 35 U.S.C. §103 over *Ishiguro et al.* and *Engineering Design Choice* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 4-5, 13-14 and 16-17 under 35 U.S.C. §103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicant respectfully requests the Examiner enters this Amendment for purposes of appeal.

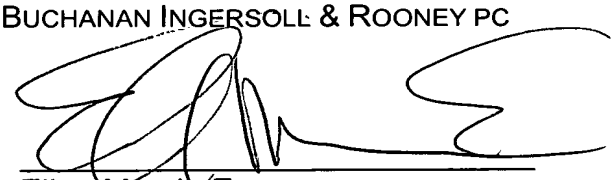
If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney a t the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: October 30, 2006 By: 

Ellen Marcie Emas
Registration No. 32131

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620